Datasheet Dynapic and Dynasim Interface-Chip DYSI-97PS/PSK/S

1 Introduction

The Interface-ASIC DYSI-97PS /S /PSK is a complex interface chip in CMOS technology. It is especially designed to condition Dynapic and Dynasim signals. 1 up to 8 signals may be conditioned with one IC. Multiple circuits can be connected together to have more than 8 inputs. There are three different package options:

- the DYSI-97PS, supplied in SOIC28, MS-013-AE, has all options, particularly all 8 parallel outputs and one serial input and one serial output (in all applications with the DYSI-97PS the DYSI-97PSK can also be implemented),
- the DYSI-97PSK, supplied in QSOP/SSOP28, MO-137-AF, has all options, particularly all 8 parallel outputs and one serial input and one serial output,
- the DYSI-97S, supplied in SO16N, MS-012-AC, has only a serial output.

2 Applications

The Interface-ASIC DYSI-97PS/PSK/S is especially useful in applications that meet one or more of the following conditions:

- For Dynapic, if long-term mode is necessary.
- For Dynapic, in the case that a debouncing is necessary.
- For Dynapic, if there are different Dynapic elements, or if more than one Dynapic element per key is used.
- For Dynasim, because the Dynasim signals are in general much weaker than the Dynapic signals and for this reason it is difficult to process these signals without a special circuit.

3 Description

3.1 General description

- When the power is applied to the DYSI-97, the internal RESET is activated. All counters are set to 0 and all inputs are shorted to VSS for 55ms. Then the circuit begins to run under normal conditions.
- The 8 Dynapic and Dynasim inputs are internal switched with current source towards VDD and with current sinks toward VSS=0V. With the connected elements (Dynapic/Dynasim) the inputs will be regulated to the constant level of „V_{GUARD}“ = 0,6V. The inputs are scanned every 1.7ms and the number of positive states are summed up. Every 7 scans the counter is compared, and if it holds 6 or 7, then a “1“-signal is passed on to the debouncing circuit. The debouncing circuit output changes its state to a “1“ after 3 successive “1“ signals, or to a “0“ after 3 successive “0“ signals . Once an output is active, the related current source and the current sink are turned off, until the output switches back to the passive logical state or until the time limit of 24s has run out. The effect of the switching off of the current sources and the current sinks is that no charges are used on the related outputs any more. Consequently a positive voltage can remain on the outputs, which leads to the hold of the activated state („long-time“). This switching off of the current sources and the current sinks can be reduced to approximately 0.2s by activating the input “TLIM“. If after reactivating the current source/sinks the inputs are still on, these inputs will be shorted after 36s for 55ms to VSS, like the restart mode.
- The voltage threshold (0.6V) is generated inside the chip and fed out also as “GUARD“. This output, which is current limited to 4.5µA, is also an input, which can be connected with an external produced voltage, as a threshold voltage.
- The 8 output signals can be read out in parallel (active “0“), when the signal “ENABLE“ is active (“0“). Several DYSI-97PS can be connected in parallel, by connecting the related outputs together and activating the signals “ENABLE“ one by one.

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JEDEC MS-013-AE = SOIC28 = PS

SYMBOL	COMMON DIMENSIONS MIN	NOM	MAX	NOTE
A	2.35	–	2.65	
A1	0.10	–	0.30	
A2	2.05	–	2.55	
b	0.31	–	0.51	7,8
b1	0.27	–	0.48	7,8
c	0.20	–	0.33	7
c1	0.20	–	0.30	7
E	10.30 BSC			
E1	7.50 BSC			3,4
e	1.27 BSC			
L	0.40	–	1.27	
L1	1.40 REF			
L2	0.25 BSC			
R	0.07	–	–	
R1	0.07	–	–	
h	0.25	–	0.75	9
θ	0°	–	8°	
θ1	5°	–	15°	
θ2	0°	–	–	
NOTE	1,2			
REF	11–614s			
ISSUE	D			

SYMBOL	TOLERANCES OF FORM AND POSITION	NOTE
aaa	0.10	
bbb	0.33	
ccc	0.10	
ddd	0.25	
eee	0.10	
fff	0.20	
NOTE	1,2	
REF	11–614s	
ISSUE	D	

VARIATION	SYMBOL D	N	REFERENCE	ISSUE
AA	10.30 BSC	16	11.3–111	A
AB	11.55 BSC	18	11.3–111	A
AC	12.80 BSC	20	11.3–111	A
AD	15.40 BSC	24	11.3–111	A
AE	17.90 BSC	28	11.3–111	A
AF	9.00 BSC	14	11.4–225	B
NOTES	3,4	6		

JEDEC MO-137-AF = QSOP/SSOP28 = PSK

COMMON DIMENSIONS AND TOLERANCES

SYMBOL	ALL DIMENSIONS IN INCHES MIN	NOM	MAX	NOTE
A	0.053	–	0.069	
A1	0.004	–	0.010	
A2	0.049	–	0.065	
b	0.008	–	0.012	7,8
b1	0.008	0.010	0.011	7,8
c	0.006	–	0.010	7
c1	0.006	0.008	0.009	7
E	0.236 BSC			
E1	0.154 BSC			3,4
e	0.025 BSC			
L	0.016	–	0.050	
L1	0.041 REF			
L2	0.010 BSC			
R	0.003	–	–	
R1	0.003	–	–	
h	0.010	–	0.020	9
θ	0°	–	8°	
θ1	5°	–	15°	
θ2	0°	–	–	
NOTE	1,2			
REF	11,11–627			
ISSUE	B			

SYMBOL	TOLERANCES OF FORM AND POSITION	NOTE
aaa	0.004	
bbb	0.008	
ccc	0.004	
ddd	0.007	
eee	0.004	
NOTE	1,2	
REF	11,11–627	
ISSUE	B	

VARIATION	SYMBOL D	N	REFERENCE	ISSUE
AA	0.193 BSC	14	11,11–627	B
AB	0.193 BSC	16	11,11–627	B
AC	0.341 BSC	18	11,11–627	B
AD	0.341 BSC	20	11,11–627	B
AE	0.341 BSC	24	11,11–627	B
AF	0.390 BSC	28	11,11–627	B
NOTES	3,4	6		

JEDEC MS-012-AC = SOIC16N = S

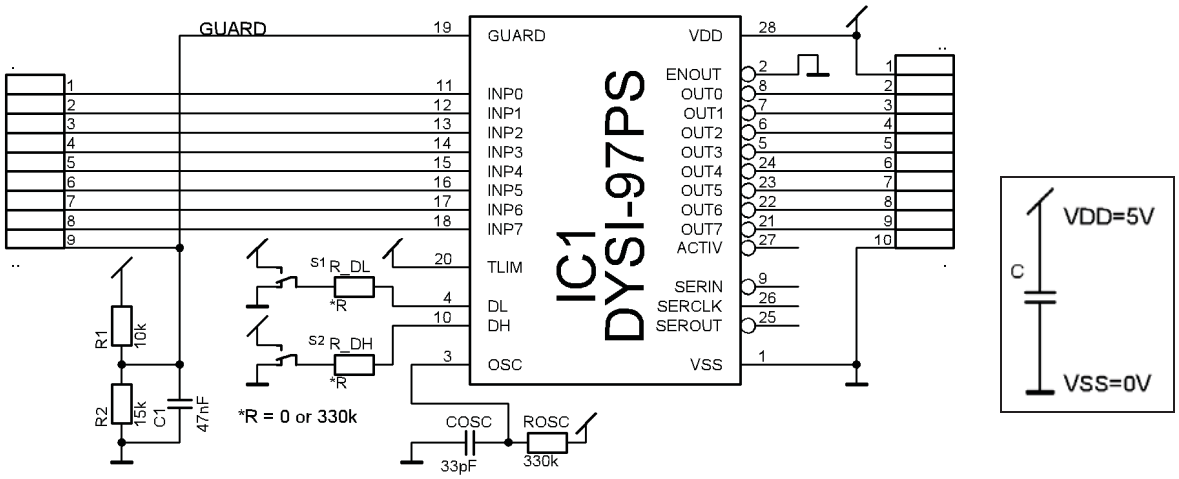
SYMBOL	COMMON DIMENSIONS MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
A2	1.25	–	1.65	
b	0.31	–	0.51	7,8
b1	0.28	–	0.48	7,8
c	0.17	–	0.25	7
c1	0.17	–	0.23	7
E	6.00 BSC			
E1	3.90 BSC			3,4
e	1.27 BSC			
L	0.40	–	1.27	
L1	1.04 REF			
L2	0.25 BSC			
R	0.07	–	–	
R1	0.07	–	–	
h	0.25	–	0.50	9
θ	0°	–	8°	
θ1	5°	–	15°	
θ2	0°	–	–	
NOTE	1,2			
REF	11–613s			
ISSUE	D			

SYMBOL	TOLERANCES OF FORM AND POSITION	NOTE
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	
eee	0.10	
NOTE	1,2	
REF	11–613s	
ISSUE	D	

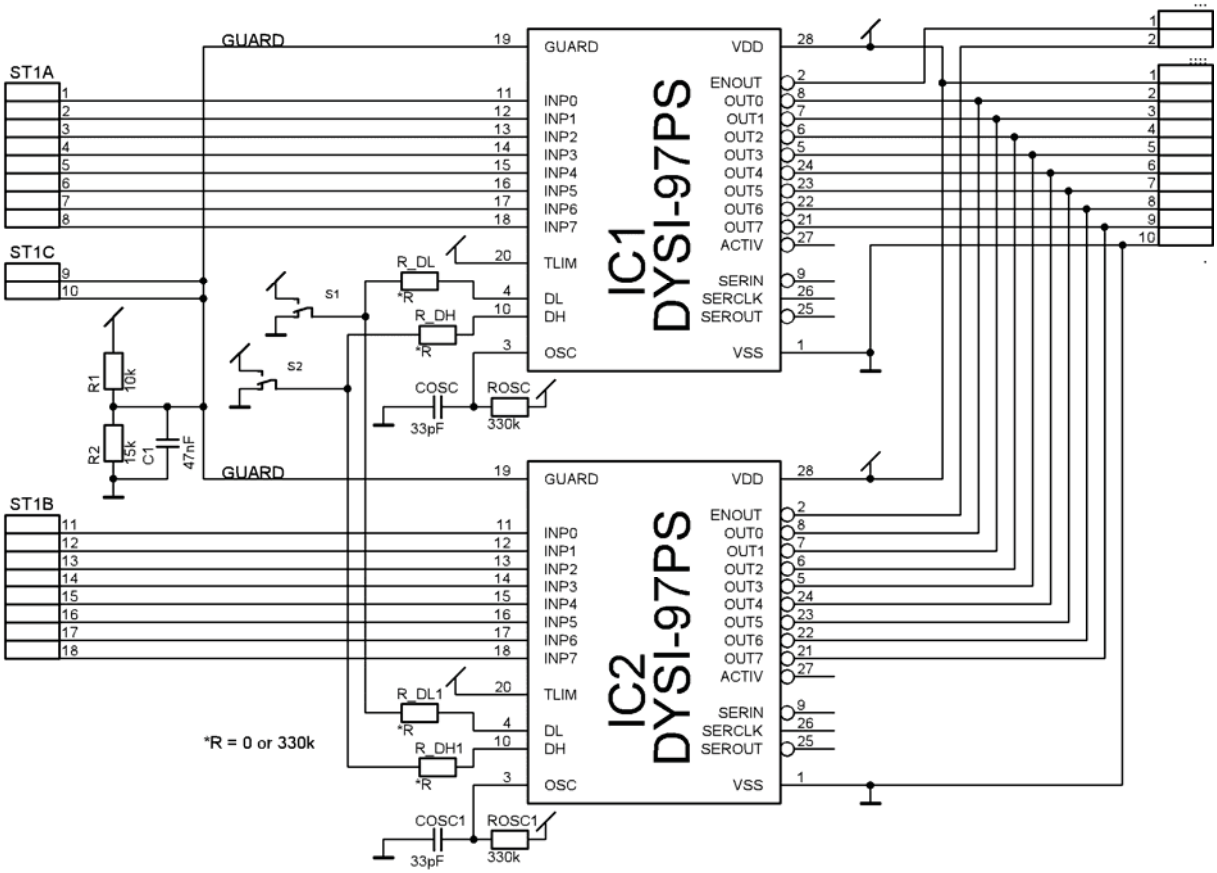
VARIATION	SYMBOL D	N	REFERENCE	ISSUE
AA	4.90 BSC	8	11.3–103	A
AB	8.65 BSC	14	11.3–103	A
AC	9.90 BSC	16	11.3–103	A
NOTES	3,4	6		

5 Examples

5.1 Example for 8 signals with a parallel output Dynapic



5.2 Example for more than 8 signals with a parallel output Dynapic



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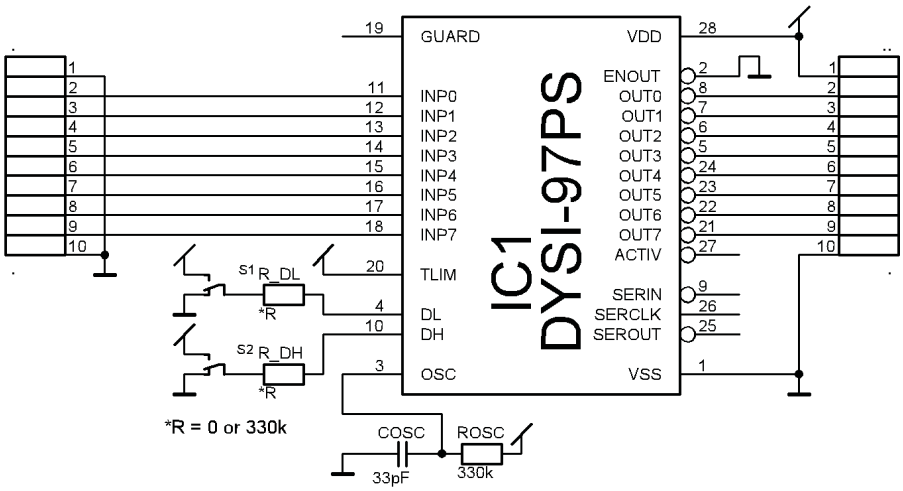
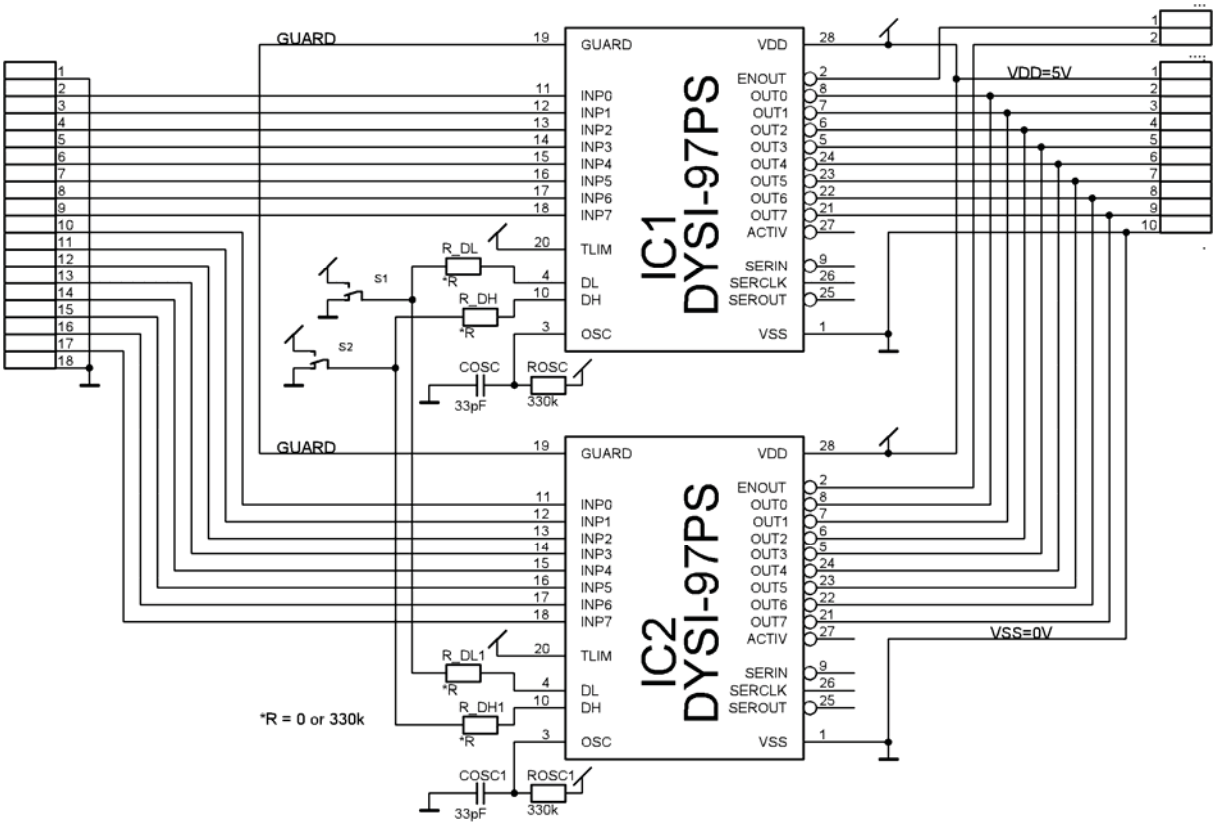
5.3 Example for 8 signals with a parallel output Dynasim



5.4 Example for more than 8 signals with a parallel output Dynasim



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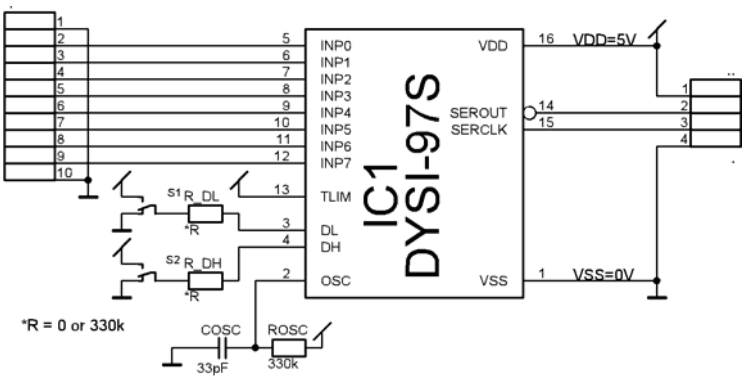
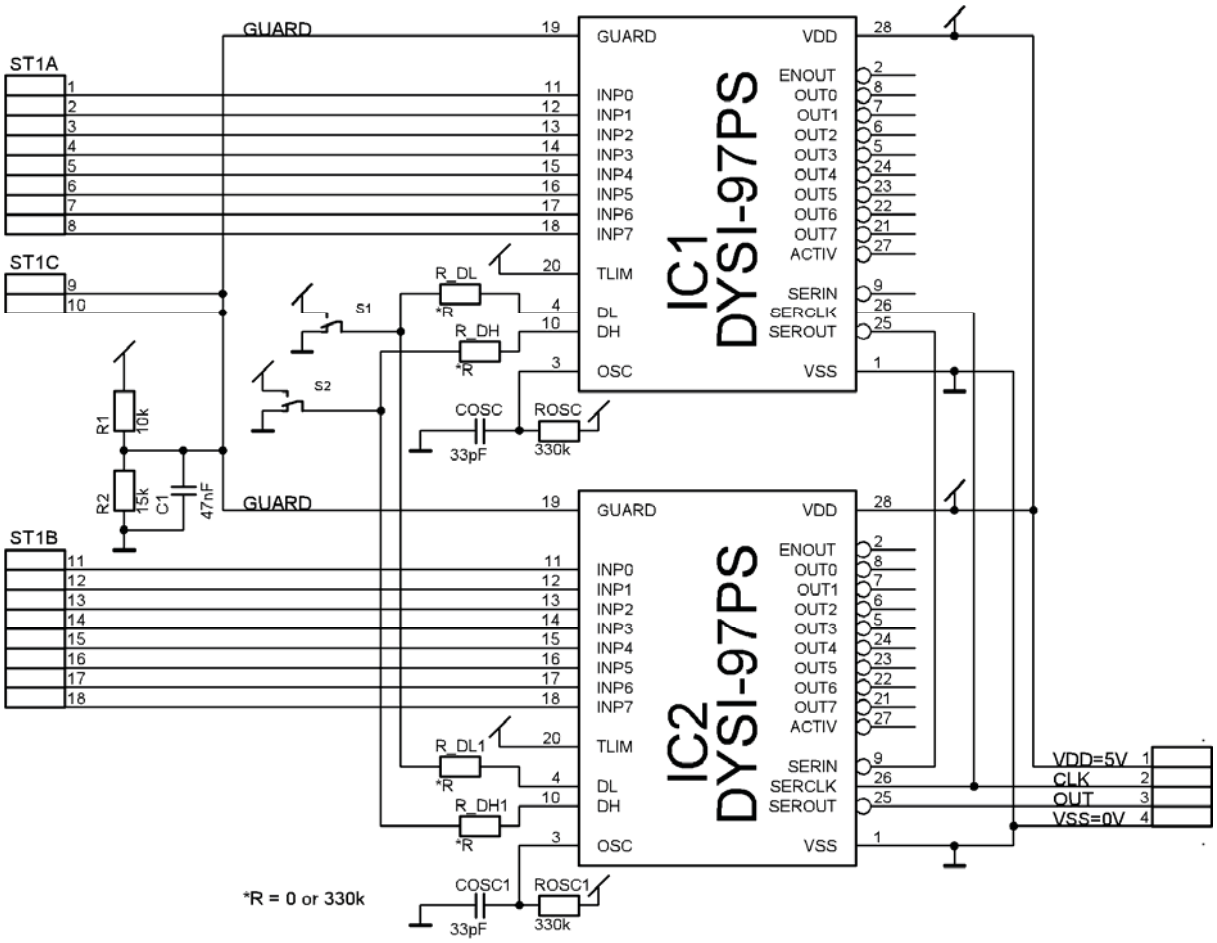
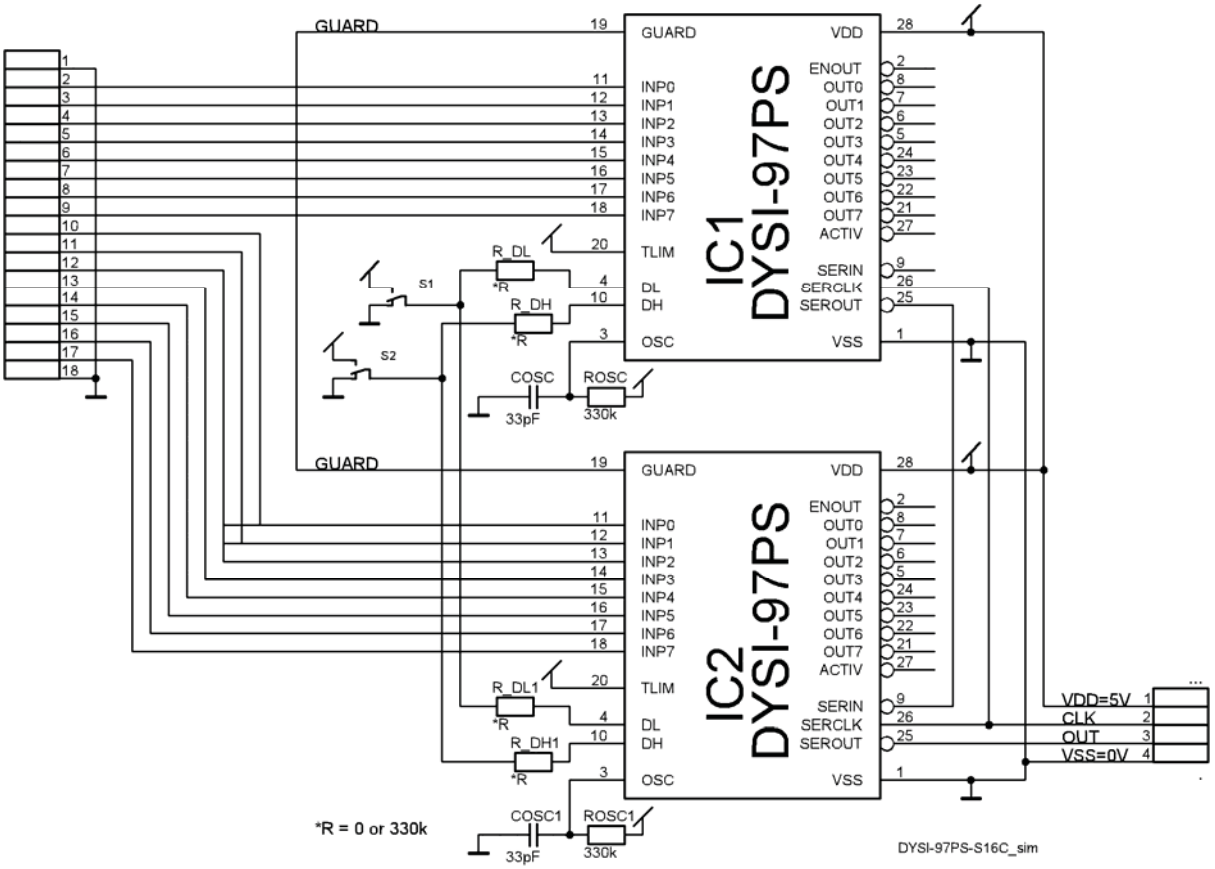
5.5 Example for 8 signals with a serial output Dynapic and Dynasim



5.6 Example for more than 8 signals with a serial output Dynapic



5.7 Example for more than 8 signals with a serial output Dynasim



6 Optional circuits

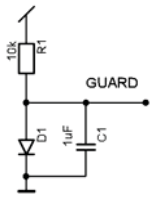
6.1 Optimization of the EMC behavior

6.1.1 Changing of the oscillator frequency

If the standard circuit of the DYSI-97 is not EMC-stable enough, the oscillator frequency can be reduced. For this purpose the oscillator R_{OSC} is increased from 330kΩ to 470kΩ, so the frequency is reduced from 75 kHz to approx. 52 kHz. This causes a rise of the thresholds and debouncing time of approx. 40%. The advantage of this circuit is that it becomes electrically more robust, without influencing the hardness of the keys tangibly. But the keys can not be activated by a short knock/pressing any more.

6.1.2 Changing of the guard circuit

In certain applications the circuit of the guard line, which is lead to the keyboard, proves to be not EMC-stable enough. In these cases the following circuit can be an improvement.

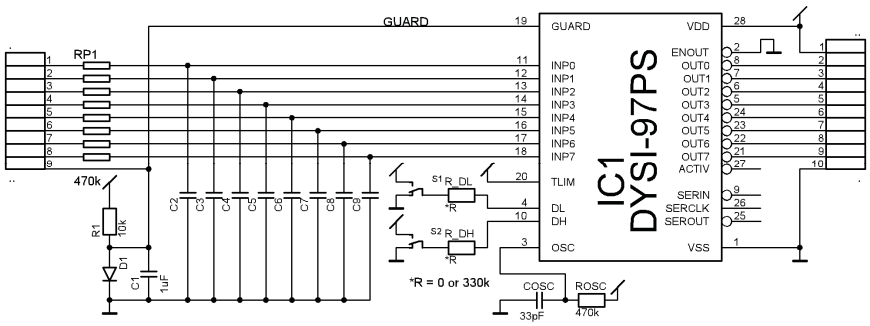


The diode D1 can be a single signal diode, several signal diodes or a Z-Diode. The voltage GUARD should be between 0.7 V and 3 V.

6.1.3 Adding of capacitors

In certain applications the circuit of the signal inputs with capacitors and/or resistances can be necessary.

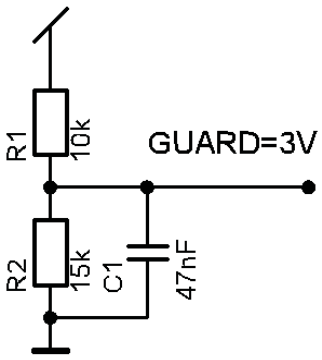
The following scheme shows a circuit with all the above mentioned optional EMC improvements.



6.2 Optional circuit only for Dynapic

If a Dynapic key is pressed very hardly, on certain conditions (high voltage signal) the circuit DYSI-97 can produce long-time signals. This effect is caused by the fact that the diode protecting the input discharges electricity towards 0V, if the input voltage becomes approx. 0,4V more negative than VSS=0V. Thereby the piezo element is charged positively and this charging can be valued as a signal. This effect can be avoided extensively by one of the following two measures.

1. The guard voltage is increased, e.g. to 3V. Consequently the quiescent voltage on the inputs is also increased from 0,6V to 3V and an input diode is only conductive when the signal voltage is more negative than approx. 3,4V, related to the guard voltage. At the same time the guard voltage is used as a common conductor for the keyboard, so that in quiescence no voltage lies against the piezo elements.



2. Since with the DYSI-97S the guard voltage is not available, a possible issue must be solved with the circuit of the signal inputs. Therefore a resistance of 470kΩ per input can be connected together in serial and a capacitor of 4,7nF towards VSS can be connected in parallel. On the one hand the current is limited by the input diode and on the other hand the impulse-shaped currents of the input circuits are smoothed.